TriMag™ Head

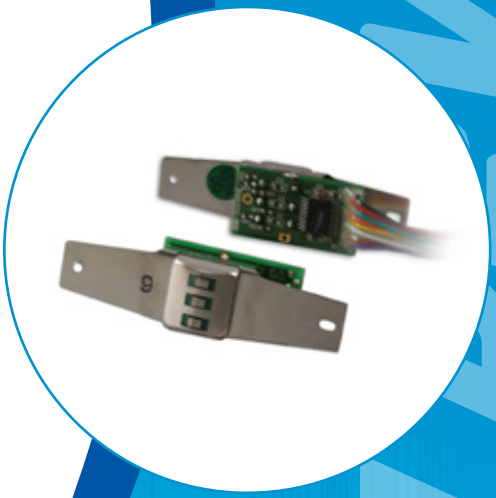
Read Head Assembly with TriMag Decoding ASIC

Magnetic Head With Triple Track Decoding Capabilities

ID TECH's TriMag™ Application-Specific Integrated Chip (ASIC) is for reading and decoding data on a magnetic stripe. Integrated onto a "read" head, the TriMag Chip Read Head Assembly delivers unsurpassed magnetic data reading reliability in a small package. The TriMag Chip is mounted directly on the read head to decode three tracks of data. The head, in turn, is mounted on a spring that provides support, spring-loaded deflection, and gimble action for great contact with the magnetic stripe. Signals from the assembly are CMOS-level outputs of decoded serial bits in either serial or clock and data formats.

Functional Description

The read head signals are amplified by the TriMag Chip using automatic gain control circuitry to ensure reliable reading. The amplified signal is used to decode the magnetic stripe data (dual-frequency using the principals of Aiken's F2F encoding) into a digital data format consisting of the magnetic stripe data, clock, and Media Detect outputs, all of which are CMOS-level signals or serial output.



Since the TriMag ASIC is mounted directly on the read head, the low amplitude analog signals are amplified and digitized without exposure to external "noise" for maximum noise immunity. TriMag technology provides reliable reading at card speeds of 3 to 80 inches per second on all three tracks of data.

The assembly's standard configuration consists of a read head, decoding chip mounted on a "wing spring," and cable assembly with a 10-pin connector for data & clock or 6-pin connector for serial output (SPI) option.

Clock & Data Output

Data/clock outputs are serial streams of digital bits with the corresponding clock for each track, which represent each data bit that was recorded on the magnetic stripe track. No data filtering is required, as the TriMag Chip automatically filters leading zeros for extraneous bits until synchronization is obtained. A data output high level is a 'ZERO' value data bit, and a low level is a 'ONE' value data bit. Data is output in Last In First Out (LIFO) sequence.

"Media Detect" for Clock & Data Output

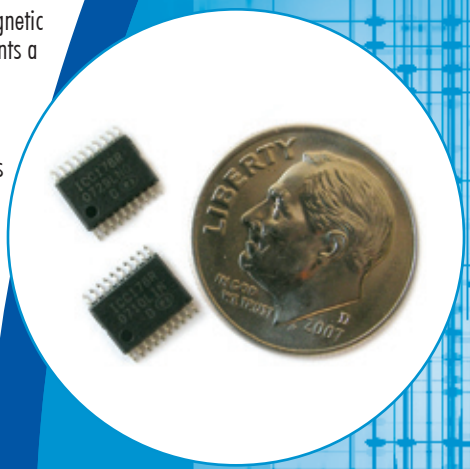
This output indicates the presence of encoded magnetic media passing the read head. This signal is normally high; a low output indicates the TriMag has determined that encoded media is being swiped. The output is an open drain type with high impedance.

SPI

Output is a single serial stream of data corresponding with the three tracks of data present on the magnetic stripe. The tracks are transmitted with track 1 first, followed by tracks 2 and 3. A high level represents a 'ONE,' when sampled on the edge of the clock.

Sleep Mode Function

The TriMag Chip will automatically enter a power-down sleep mode when a magnetic head signal is not present. The TriMag Chip will automatically wake up when a magnetic head signal is present. The data, clock, and Media Detect outputs are at a high level during sleep mode.



Features

- Low power—sleeps when not reading
- Current consumption less than 3mA typical when reading a card
- Current consumption less than 85μA per track when in "sleep" mode
- Operating voltage of 3.3V or 5V
- Provides unequalled noise immunity
- True AGC handles signal amplitudes from 1mV to 1V p-p
- Excellent data jitter, media glitch, and drop-out immunity
- ± 15KV Electro-Static Discharge (ESD) protection when head case is grounded
- Reads card swipe speeds from 3 to 80+ inches per second (7.5 to 200+ cm/sec)
- Supports bi-directional card swiping and decoding

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TriMag™ Head Specifications AHD-1303-33

Recommended Operation Conditions

Symbol	Parameter	Min	Max	Units
Vdd_5V	5.0V DC Supply	4.5	5.5	V
Vdd_3V	3.3V DC Supply	2.73	3.6	V
Iddd	Dynamic Current		3	mA
Idds5	Standby Current (5V)		70	uA
Idds3	Standby Current (3.3V)		60	uA
Avss	Analog Ground		0	V
Dvss	Digital Ground		0	V
Ta	Ambient Temperature	-40	85	C
Tj	Junction Temperature	-40	90	C

Clock & Data (ASIC)

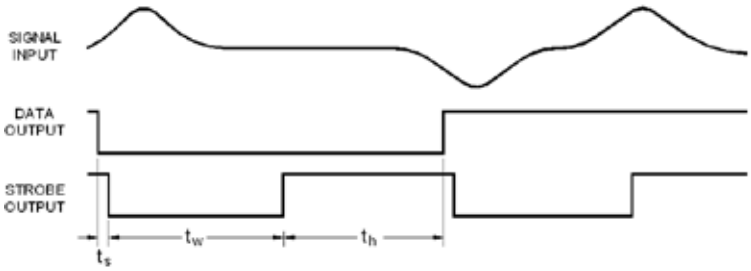
Pin #	Signal	Direction	Color
1	Signal Common	-	Black
2	Clock Output 2	Out	Gray
3	Data Output 2	Out	White
4	Media Detect	Out	Jumper
5	Clock Output 1	Out	Yellow
6	Data Output 1	Out	Orange
7	Head Case	-	Green & Jumper
8	+3V or +5V	In	Red
9	Clock Output 3	Out	Brown
10	Data Output 3	Out	Purple

Clock Output

Clocking output is normally high, and goes low to indicate a data sample time. The data output is stable and may be sampled on the falling or rising edge of the clock, or at any time while the clock is low.

The TriMag Chip clock goes low approximately 2 μsec after the data output is valid. The clock width changes with speed. The receiving interface for TriMag Chip data must sense the high-to-low clock transition and acquire the data bit level during clock pulse. The clock width changes with speed.

Clock & Data Output Diagram



Symbol	Parameter	Timing
t_s	Setup Time, DATA Change to Strobe (Clock) Falling Edge	3μS ± 50%
t_h	Strobe (Clock) Rising Edge to DATA Change	50% of bit width ±3μS
t_w	Pulse Width, Strobe (Clock)	50% of bit width ±3μS

Environmental

Operating: -35°C to 70°C (10% to 98% relative humidity).
Storage: -45°C to 85°C (10% to 98% relative humidity).

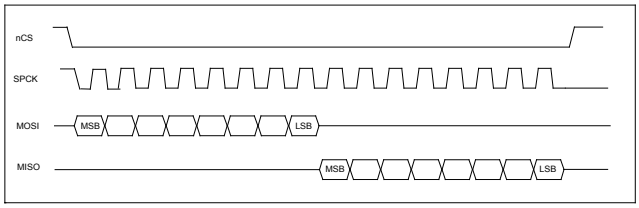
Durability

Head life is 1,000,000 card cycles (with media that meets ISO 7811 magnetic stripe properties) under a non-contaminated environment. Spring assembly is 1,000,000 card cycles as well.

SPI (Full Duplex)

Pin #	Signal	Direction	Color
1	SCLK	In	Violet
2	MOSI	In/Out	Blue
3	MISO	In/Out	Yellow
4	3V or 5V	In	Red
5	Signal Common	-	Black
6	Head Case	-	Green

SPI Transmission Waveform



SPI Operation & Outputs

The SPI operation implements a common SPI slave-only interface. Although there are many permutations of SPI, the TriMag offers only a single communication format. This format is the most common. Its characteristics are as follows:

- Input data is latched on the rising edge of the serial clock
- Output data is shifted out on the falling edge of the serial clock
- SPI is enabled when nCS is low
- Output data is tri-stated when SPI is not enabled (nCS is high)
- The maximum SPI clock rate is less than 500 kHz ensuring memory reads have sufficient time to complete for back-to-back SPI reads.

These relationships are shown above for a simple 8-bit command, followed by an 8-bit response.

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